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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,226	09/18/2003	Donald Craig Foster	AMKOR-089A	7010

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,226	FOSTER, DONALD CRAIG	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1-6 and 8-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,402,318 to Otsuka et al. and US Patent Application Publication No. 2002/0038873 to Hiyoshi.

Regarding claim 1, Otsuka et al. (figures 8-12) teach an interposer for use in a semiconductor package, the interposer comprising:

an interposer body (103) molded from a dielectric material, the interposer body (103) defining opposed top (an upper surface of 103) and bottom (a bottom surface of 103) surfaces, an outer peripheral edge (a portion of outer edge of 103), and an inner peripheral edge (a portion of inner edge of 103);

a die pad (a portion of die pad [104], which is formed under the chip [102]) having opposed top (an upper surface of the die pad [104]) and bottom (a bottom surface of the die pad [104]) surfaces and a peripheral edge (a portion of peripheral edge of the die pad [104]), the inner peripheral edge of the interposer body (103) and the top surface of the die pad (104) collectively defining a cavity of the interposer; the die pad (104) being embedded within the interposer body such that the bottom surface of the die pad (a portion of die pad, which is formed

under the chip [102]) is exposed in and substantially flush with the bottom surface of the interposer body (103).

Otsuka et al. differ from the claimed invention by not showing a plurality of electrically conductive interposer leads embedded within the top surface of the interposer body and at least partially exposed therein, each of the interposer leads defining a land; and the interposer body forming a non-conductive barrier between each of the interposer leads and between the interposer leads and the die pad. However, Hiyoshi (figure 8) shows a plurality of electrically conductive (wiring [51]) formed on the top surface of the die pad (the die pad is formed under the chip [33]), and defined a land, and the non-conductive barrier layer (insulation resin [14]) formed between the conductive layer (51) and the die pad. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hiyoshi into the device taught by Otsuka et al. because it the leads provide interconnections in the semiconductor package.

Regarding claim 2, the combined device shows each of the interposer leads (Hiyoshi; [51]) includes a finger portion having a top surface, which is exposed (a portion of [51] is exposed) in and substantially flush with the top surface of the interposer body.

Regarding claim 3, the combined device shows the finger portion of each of the interposer leads (Hiyoshi; a portion of [51]) has an interior terminal end (a right portion of [51]) which extends to the cavity and an exterior terminal end (a left portion of [51]) which extends beyond the outer peripheral edge of the interposer body; and each of the interposer leads (Hiyoshi; a portion of [51]) further includes a protuberance which projects downwardly (a portion of [51] is downwardly from the finger portion of [51) from the finger portion in close proximity to the

exterior terminal end thereof the protuberance being oriented outward of the outer peripheral edge of the interposer body and defining the land.

Regarding claim 4, the combined device shows the land of each of the interposer leads (Hiyoshi; 51), the bottom surface of the die pad (Otsuka et al.; 104), and the bottom surface of the interposer body extend in generally co-planar relation to each other.

Regarding claim 5, the combined device shows the finger portion of each of the interposer leads (Hiyoshi; 51) has an interior terminal end which extends to the cavity and an exterior terminal end which extends beyond the outer peripheral edge of the interposer body; and each of the interposer leads (Hiyoshi; 51) includes a downset which is formed within the finger portion thereof in close proximity to the exterior terminal end, the downset being partially covered by the interposer body and defining the land which is exposed in the bottom surface of the interposer body.

Regarding claim 6, the combined device shows the land of each of the interposer leads, the bottom surface of the die pad, and the bottom surface of the interposer body extend in generally co-planar relation to each other.

Regarding claim 8, the combined device shows a plurality of package leads supported by at least one of the interposer body and the interposer leads; a semiconductor die attached to the top surface of the die pad and electrically connected to at least some of the interposer leads and the package leads; and a package body (Otsuka et al.; 116) at least partially covering the semiconductor die (Otsuka et al.; 102), the interposer and the package leads such that at least portions of the package leads, the lands of the interposer leads and the bottom surface of the die pad are exposed in the package body.

Regarding claim 9, the combined device shows the lands and the bottom surface of the die pad are exposed in and substantially flush with a bottom surface of the package body, and portions of the package leads protrude from respective side surfaces of the package body.

Regarding claim 10, the combined device shows the lands, the bottom surface of the die pad, and portions of the package leads are exposed in and substantially flush with a bottom surface of the package body.

Regarding claim 11, Otsuka et al. (figures 8-12) teach an interposer for use in a semiconductor package, the interposer comprising:

a die pad (a portion of die pad 103, which is formed under the chip 102) having opposed top (an upper surface of the die pad) and bottom (a bottom surface of the die pad) surfaces and a peripheral edge;

a layer of adhesive tape (a portion of the adhesive layer; column 7, lines 15-18) attached to the top surface of the die pad, the layer and the top surface of the die pad collectively defining a cavity of the interposer.

Otsuka et al. differ from the claimed invention by not showing a plurality of electrically conductive interposer leads embedded within the top surface of the interposer body and at least partially exposed therein, each of the interposer leads defining a land. However, Hiyoshi (figure 8) shows a plurality of electrically conductive (51) formed on the top surface of the die pad (the die pad is formed under the chip [33]), and defined a land. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hiyoshi into the device taught by Otsuka et al. because it the leads provide interconnections in the semiconductor package.

Regarding claim 12, the combined device shows each of the interposer leads (Hiyoshi; [51]) includes a finger portion (Hiyoshi; a portion of [51]) having a top surface (Hiyoshi; an upper surface of [51]) which extends in spaced, generally parallel relation to the top surface (Otsuka et al.; an upper surface of the die pad [104]) of the die pad and is electrically isolated therefrom by the layer of adhesive tape (a portion of the adhesive; column 7, lines 15-18).

Regarding claim 13, the disclosures of Otsuka et al. and Hiyoshi are discussed as applied to claim 3 above.

Regarding claim 14, the disclosures of Otsuka et al. and Hiyoshi are discussed as applied to claim 4 above.

Regarding claim 15, the disclosures of Otsuka et al. and Hiyoshi are discussed as applied to claim 5 above.

Regarding claim 16, the disclosures of Otsuka et al. and Hiyoshi are discussed as applied to claim 6 above.

Regarding claim 17, the disclosures of Otsuka et al. and Hiyoshi are discussed as applied to claim 8 above.

Regarding claim 18, the disclosures of Otsuka et al. and Hiyoshi are discussed as applied to claim 9 above.

Regarding claim 19, the disclosures of Otsuka et al. and Hiyoshi are discussed as applied to claim 10 above.

Regarding claim 20, Otsuka et al. (figures 8-12) teach an interposer for use in a semiconductor package, the interposer comprising:

a die pad (a portion of the die pad, which is formed under the chip 102) having opposed top (an upper surface of the die pad 104) and bottom (a bottom surface of the die pad 104) surfaces and a peripheral edge;

Otsuka et al. differ from the claimed invention by not showing a plurality of electrically conductive interposer leads embedded within the top surface of the interposer body and at least partially exposed therein, each of the interposer leads defining a land; and the interposer body forming a non-conductive barrier between each of the interposer leads and between the interposer leads and the die pad. However, Hiyoshi (figure 8) shows a plurality of electrically conductive (wiring [51]) formed on the top surface of the die pad (the die pad is formed under the chip [33]), and defined a land, and the non-conductive barrier layer (insulation resin [14]) formed between the conductive layer (51) and the die pad. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hiyoshi into the device taught by Otsuka et al. because it the leads provide interconnections in the semiconductor package.

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka et al. in view of Hiyoshi, and further in view of US Patent No. 5,637,922 to Fillion et al.

Regarding claim 7, the disclosures of Otsuka et al. and Hiyoshi are discussed as applied to claims 1-6, 8 and 10 above.

The combined device differs from the claimed invention by not showing the interposer body includes an integral pedestal, which is disposed on the top surface thereof and extends over portions of each of the interposer leads. However, Fillion et al. (figure 10) shows the pedestal

layer (26d), which is disposed on the top surface thereof and extends over portions of each of the conductive layer (24). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Fillion et al. into the device taught by Otsuka et al. and Hiyoshi because it provides a support for the semiconductor package.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
October 26, 2004

Sara Crane
Primary Examiner